

FIG. 1

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The diagram illustrates a microprocessor-based electronic device, labeled FIG. 1. The central component is a MICROPROCESSOR CENTRAL PROCESSING UNIT (12). Key functional blocks and their interconnections include:

- Power Input and Regulation:** A POWER INPUT (P) is connected to a POWER REGULATOR (14), which provides VDD to the microprocessor and other components. A POWER SWITCHING PORT (16a) is also connected to the power line.
- Control and Timing:** An OSCILLATOR provides CLOCK INPUTS to the microprocessor. A TONE GENERATING PORT (26a) is connected to the microprocessor and a HORN DRIVER CIRCUITY (26).
- Memory and Data:** ROM (12a) and RAM (12b) are connected to the microprocessor. A TONE / TEMPORAL SENSING PORT (32a) is also connected to the microprocessor.
- Input/Output and Sensing:** A SYNC PULSE & FWR SENSING PORT (14a) is connected to the microprocessor. A CHARGE DRIVER PORT (18a) is connected to the microprocessor and a CHARGING CONTROL CIRCUITY (18). A PULSE WIDTH DETECT PORT (24a) is connected to the microprocessor and a VOLTAGE TO PULSE WIDTH OPTION (24-1).
- Output and Firing:** A BULB DRIVER PORT (22a) is connected to the microprocessor and a BULB FIRING CIRCUITY (22). A MODEL SENSING PORT (30a) is connected to the microprocessor and a MODEL SELECT SWITCH (30).
- Internal Components:** IC RESET COMPONENTS are connected to the microprocessor. A VDD & INTERNAL RESET block is also connected to the microprocessor.
- External Options:** A CAP. VOLTAGE DIVIDER CIRCUITY A TO D OPTION (24-2) is connected to the microprocessor. A STORAGE CAPACITOR & FLASH BULB ELEMENTS (20-2) are connected to the microprocessor and a VOLTAGE TO PULSE WIDTH OPTION (20-1).

The diagram is labeled with various reference numerals (10, 12, 14, 16, 18, 20, 22, 24, 26, 30, 32) and includes a page number 1/13.

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FIG. 2A-1

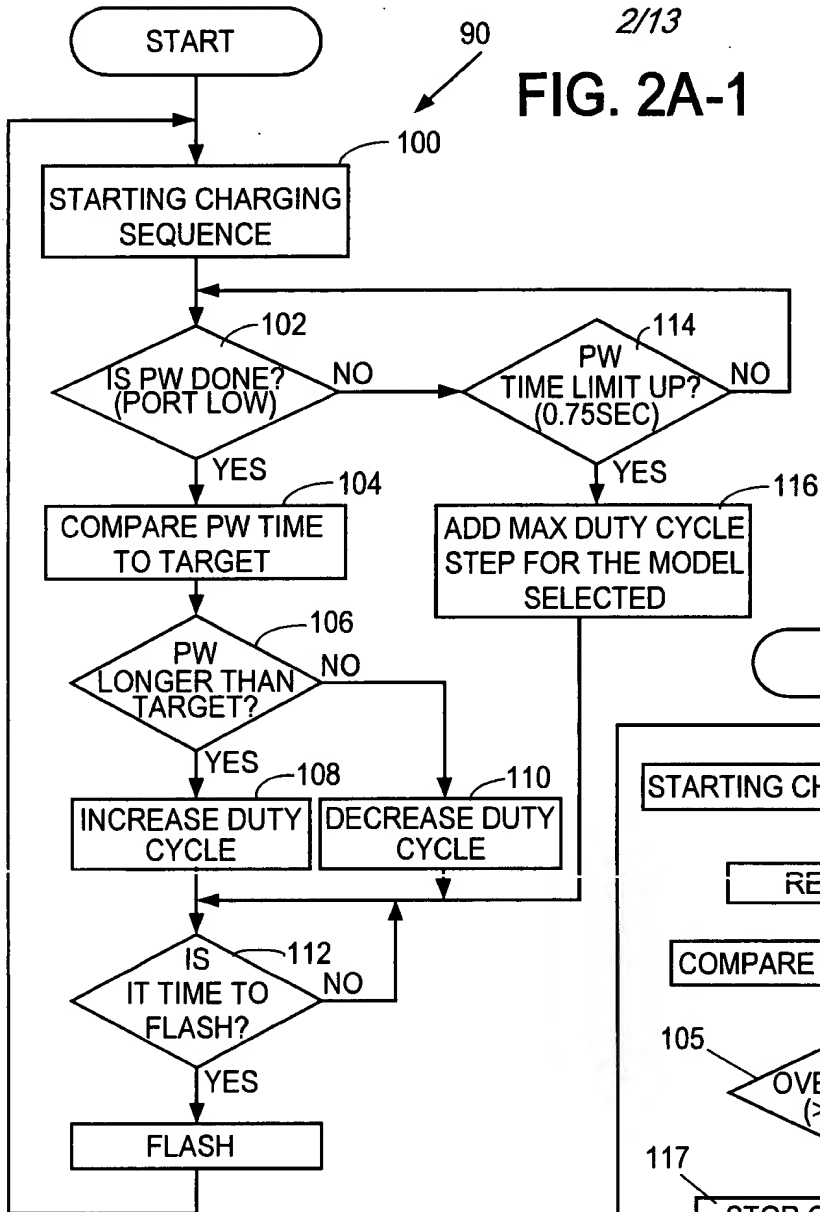
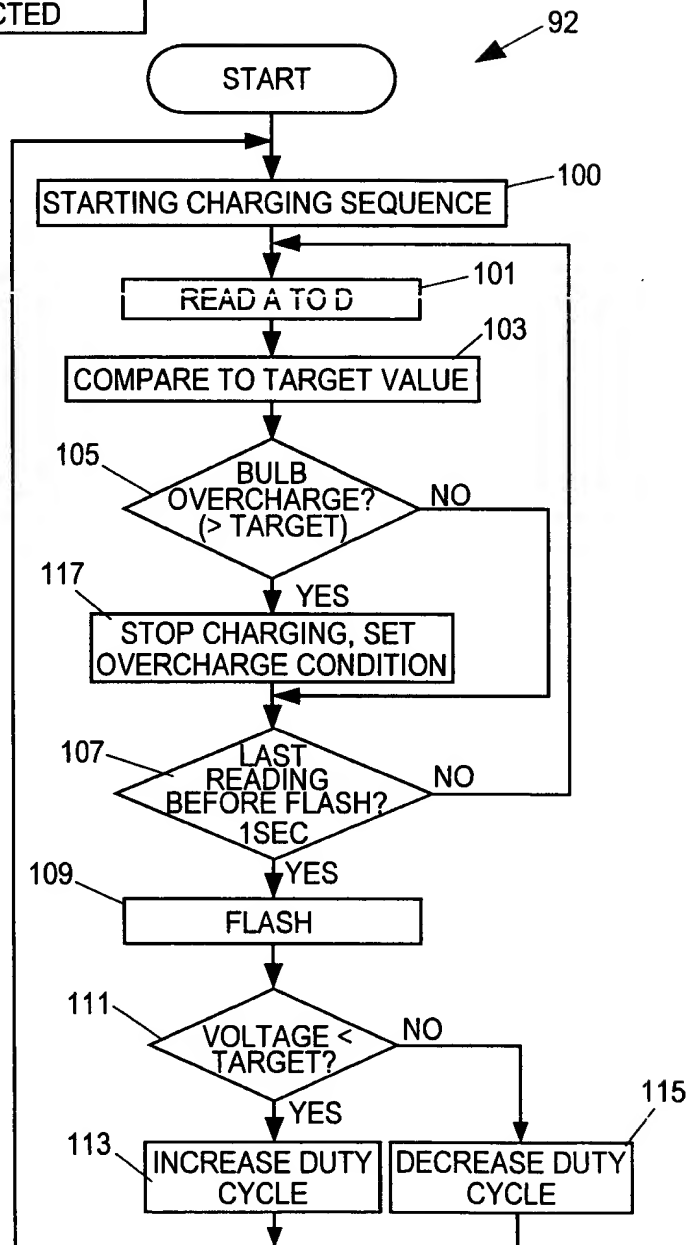
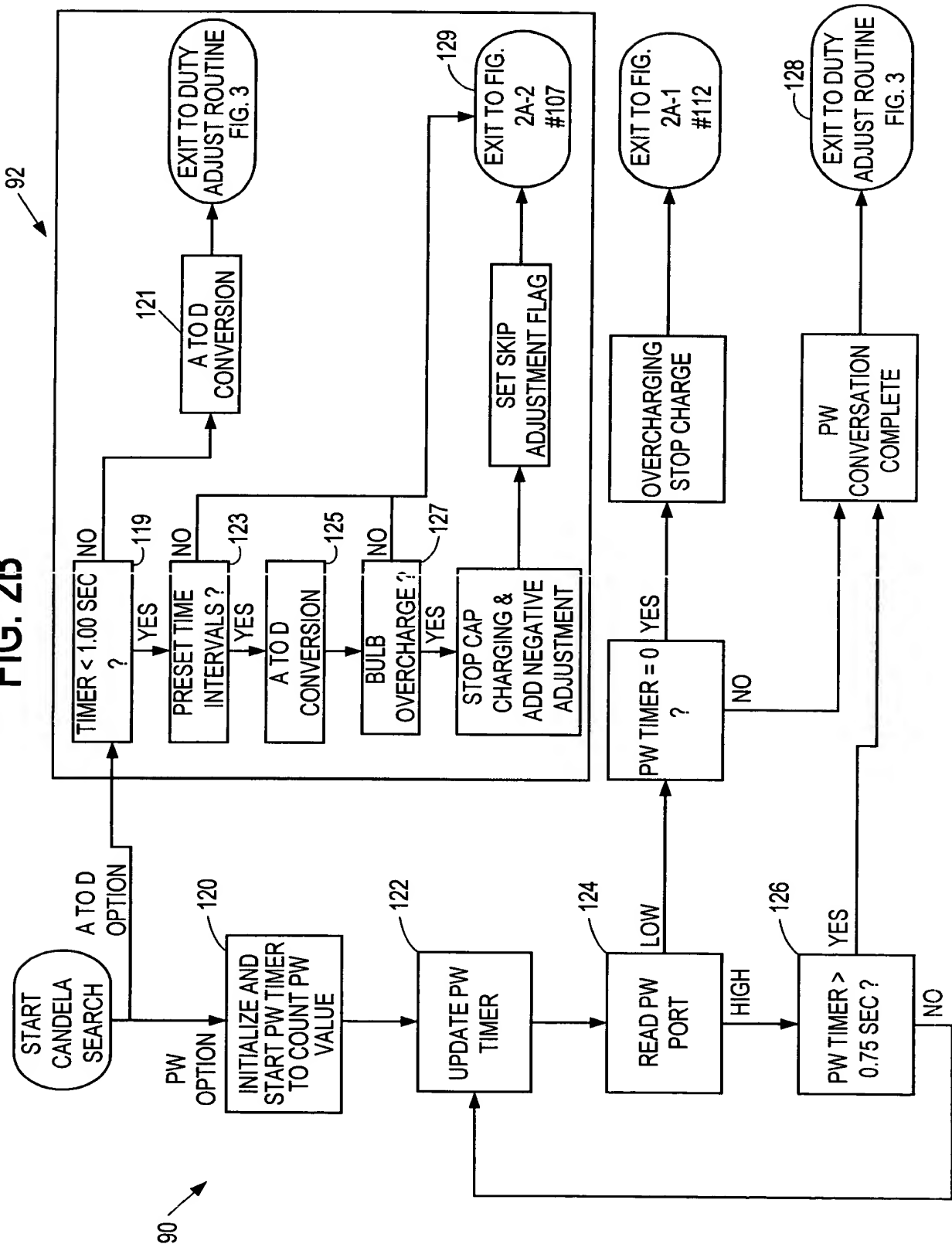


FIG. 2A-2



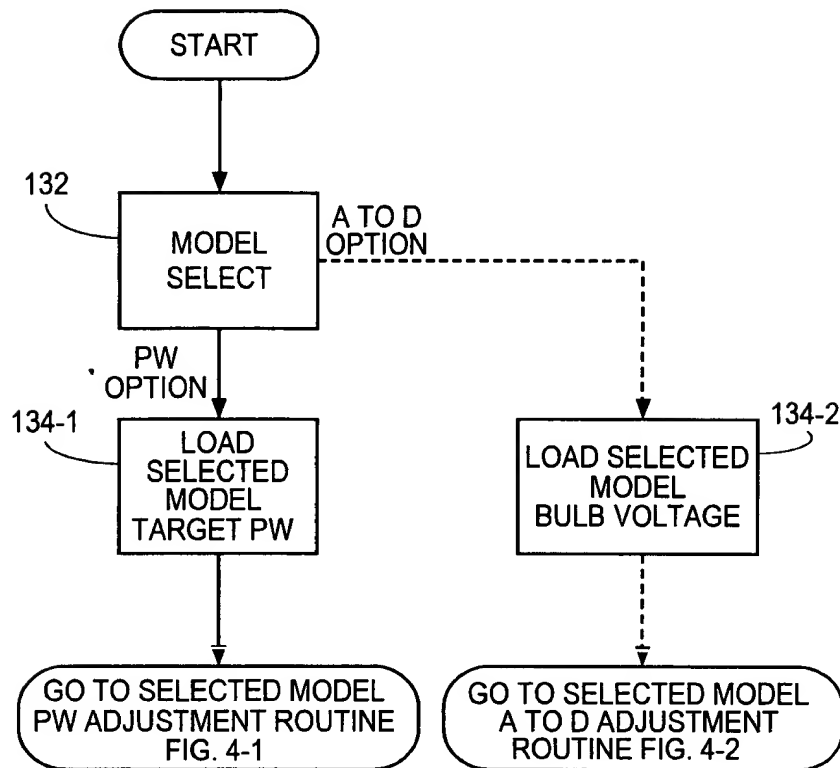
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FIG. 2B



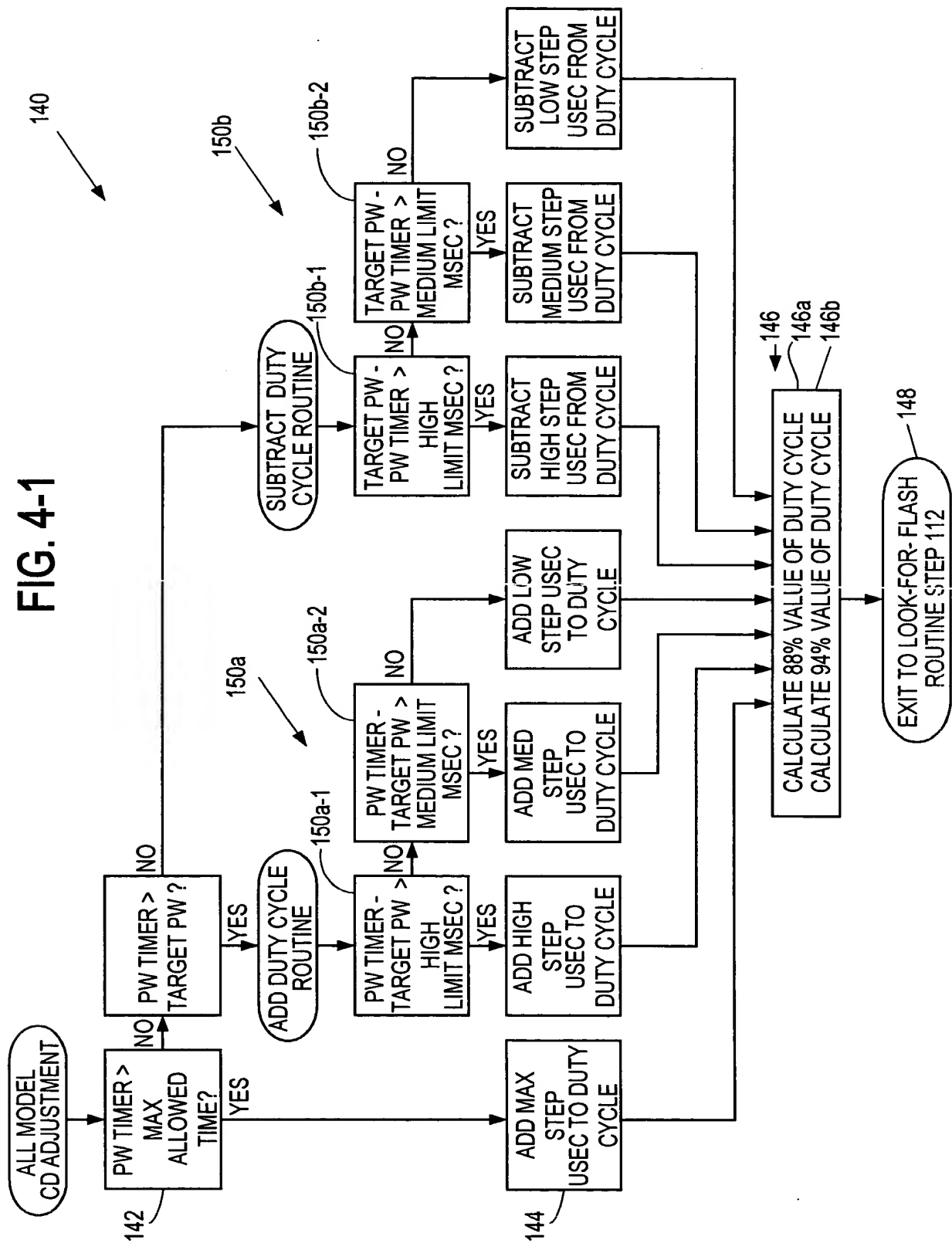
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FIG. 3



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FIG. 4-1



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FIG. 4-2

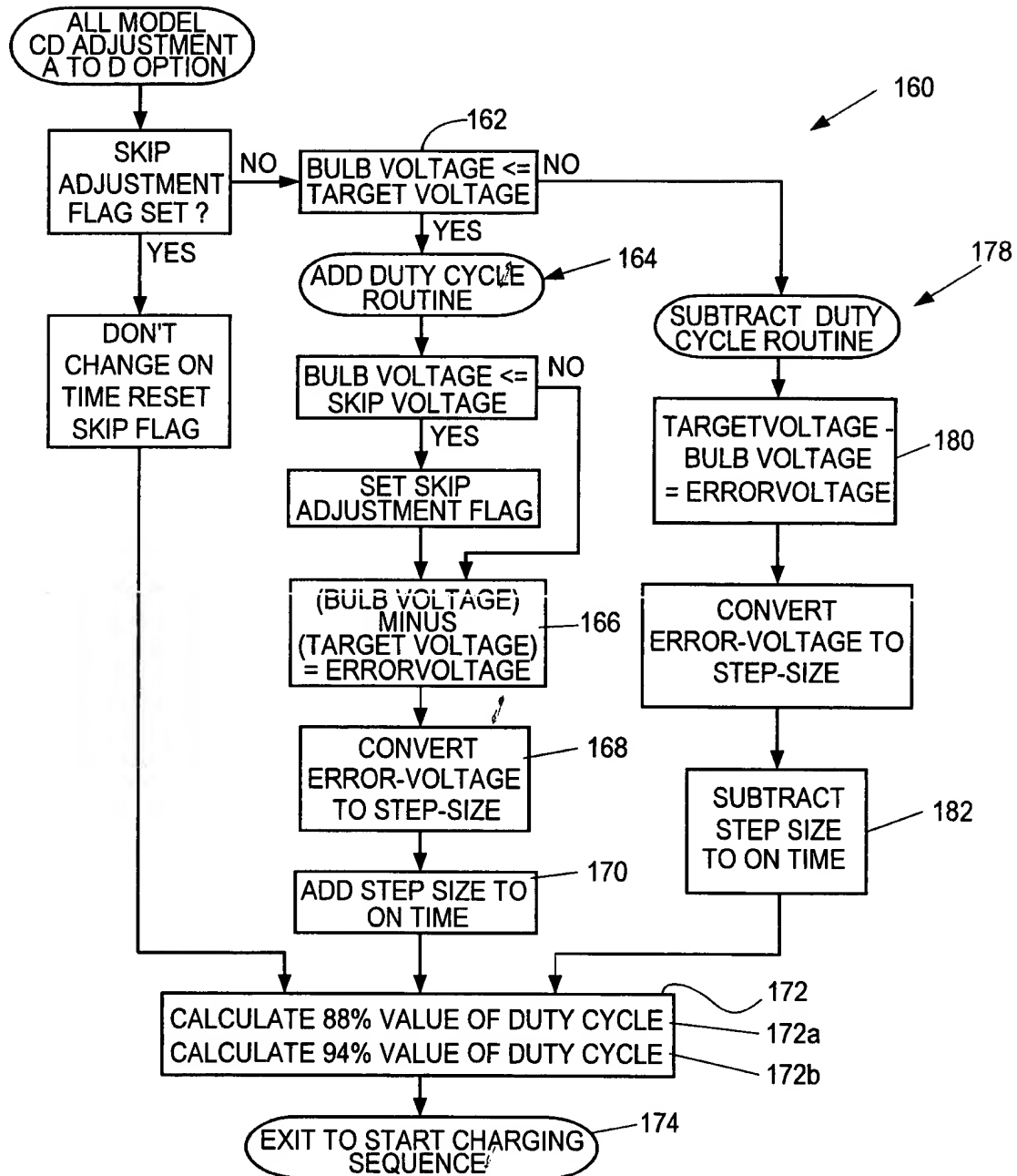


FIG. 5-1

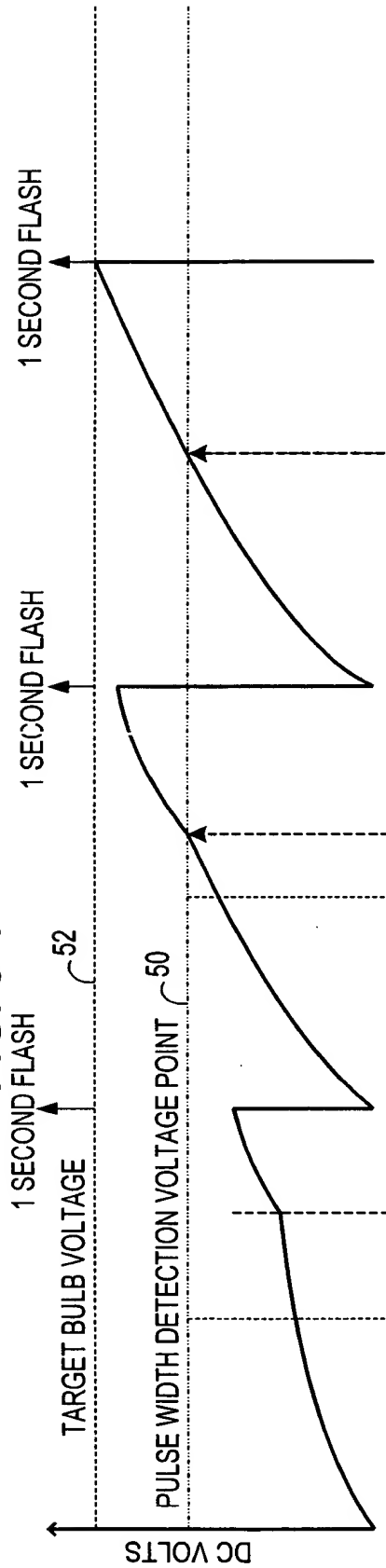


FIG. 5-2

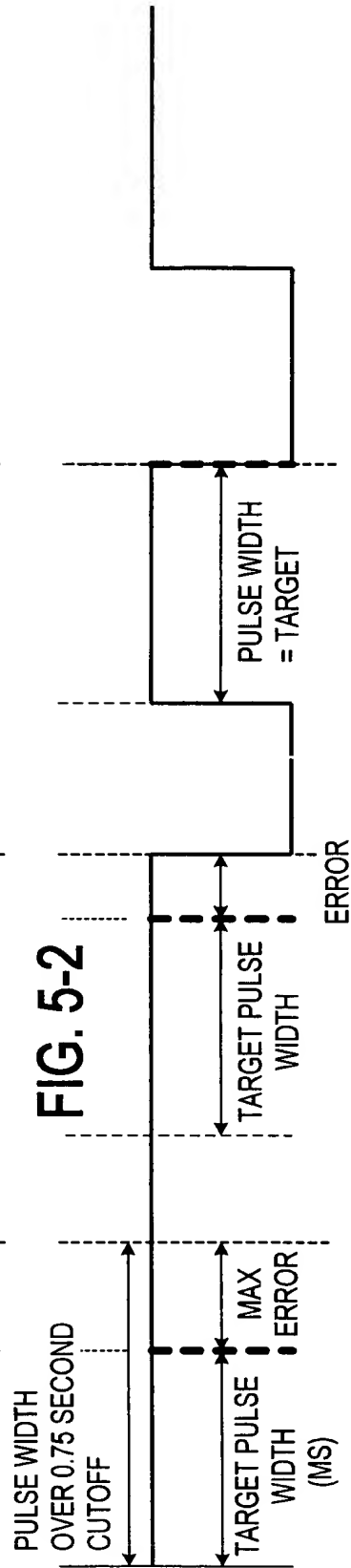
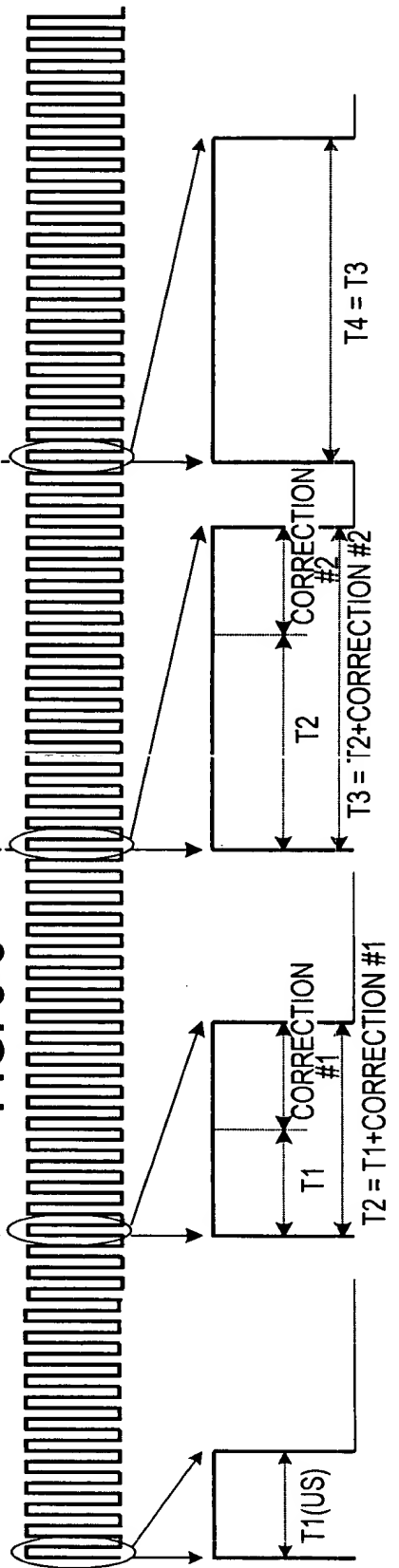


FIG. 5-3



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FIG. 6-1

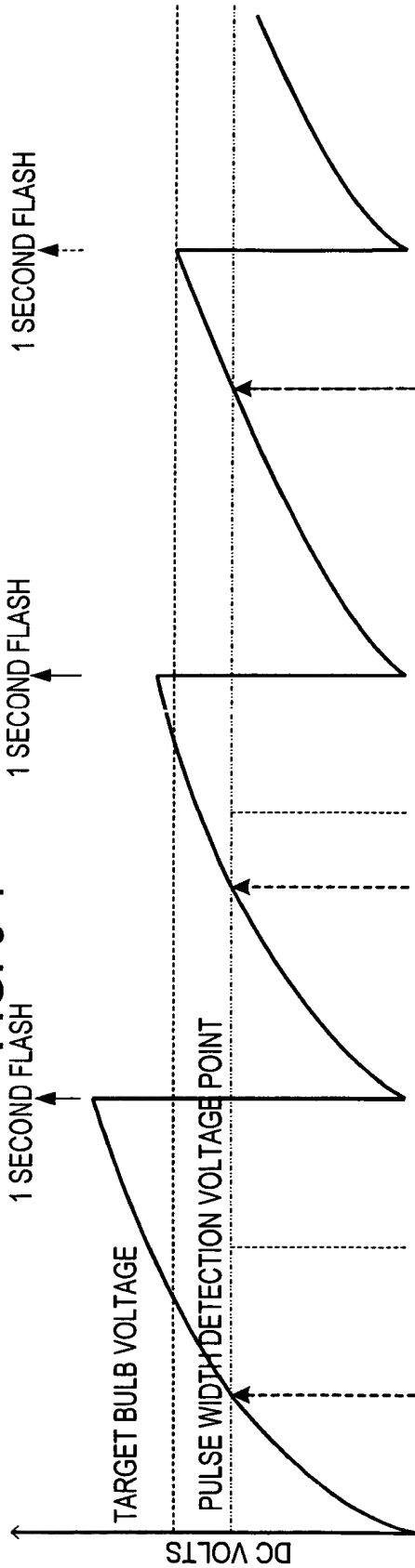


FIG. 6-2

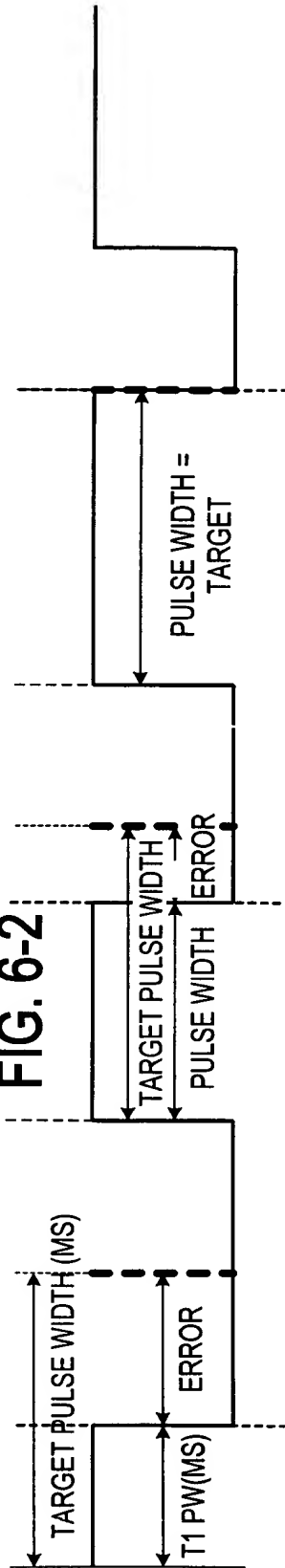
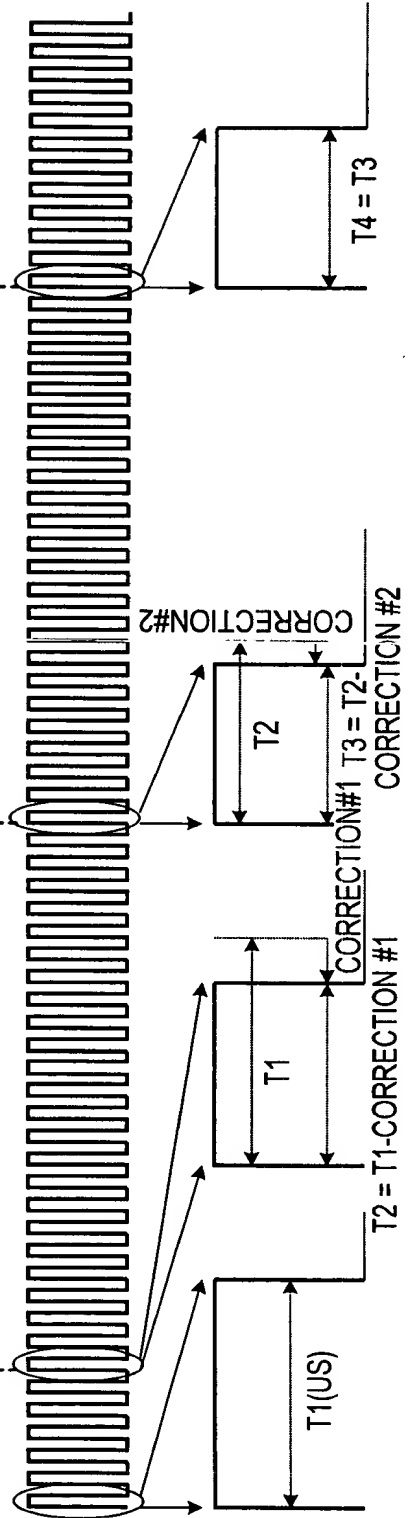


FIG. 6-3



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FIG. 7-1

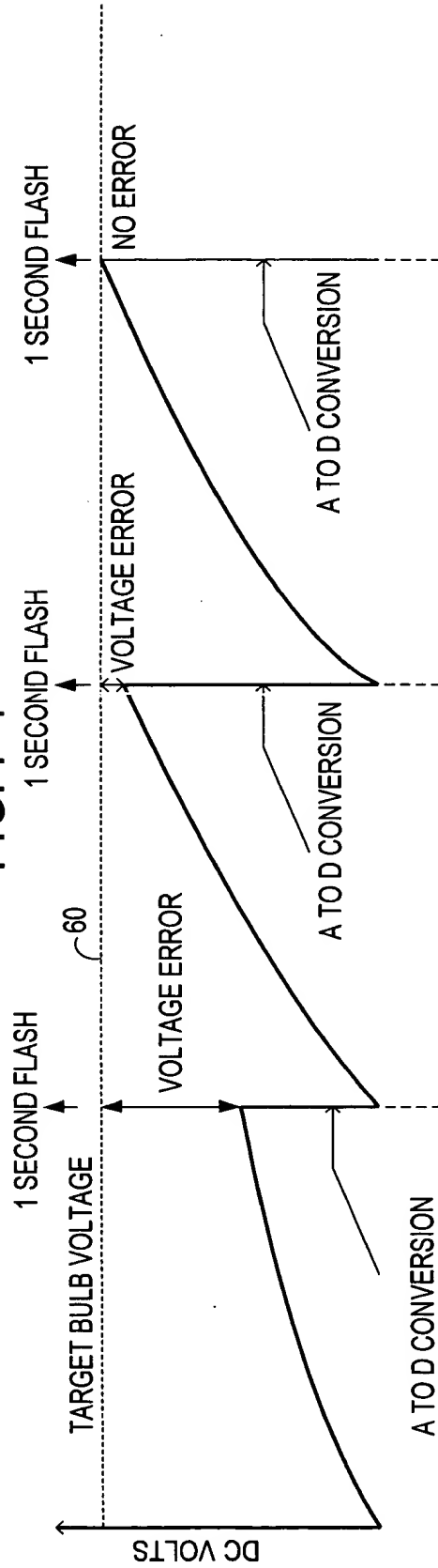
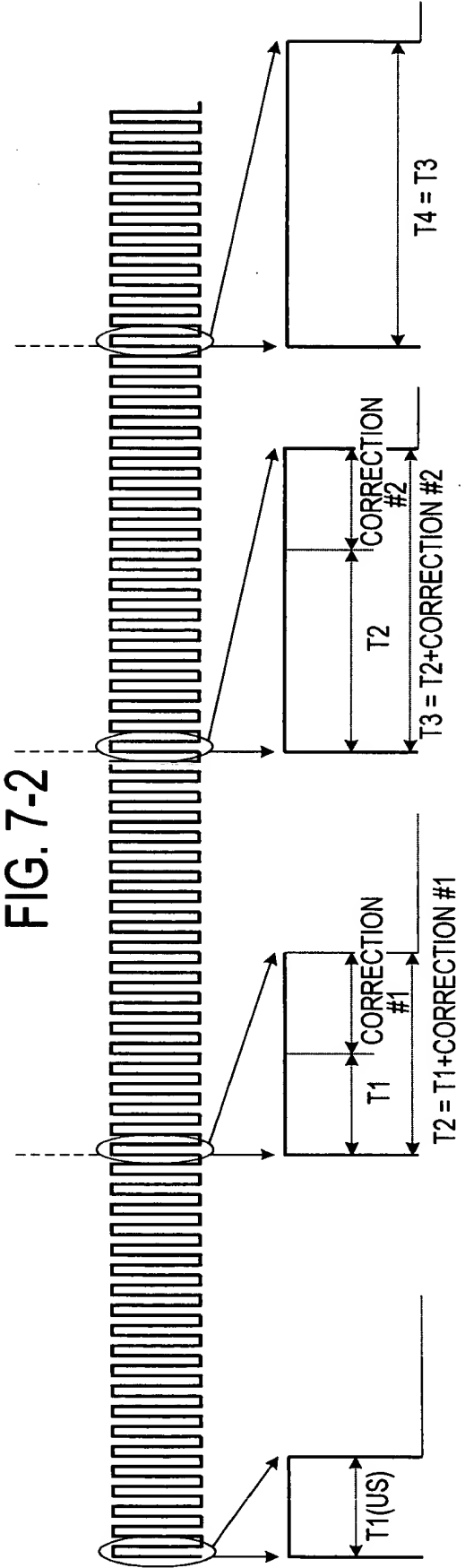


FIG. 7-2



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FIG. 8-1

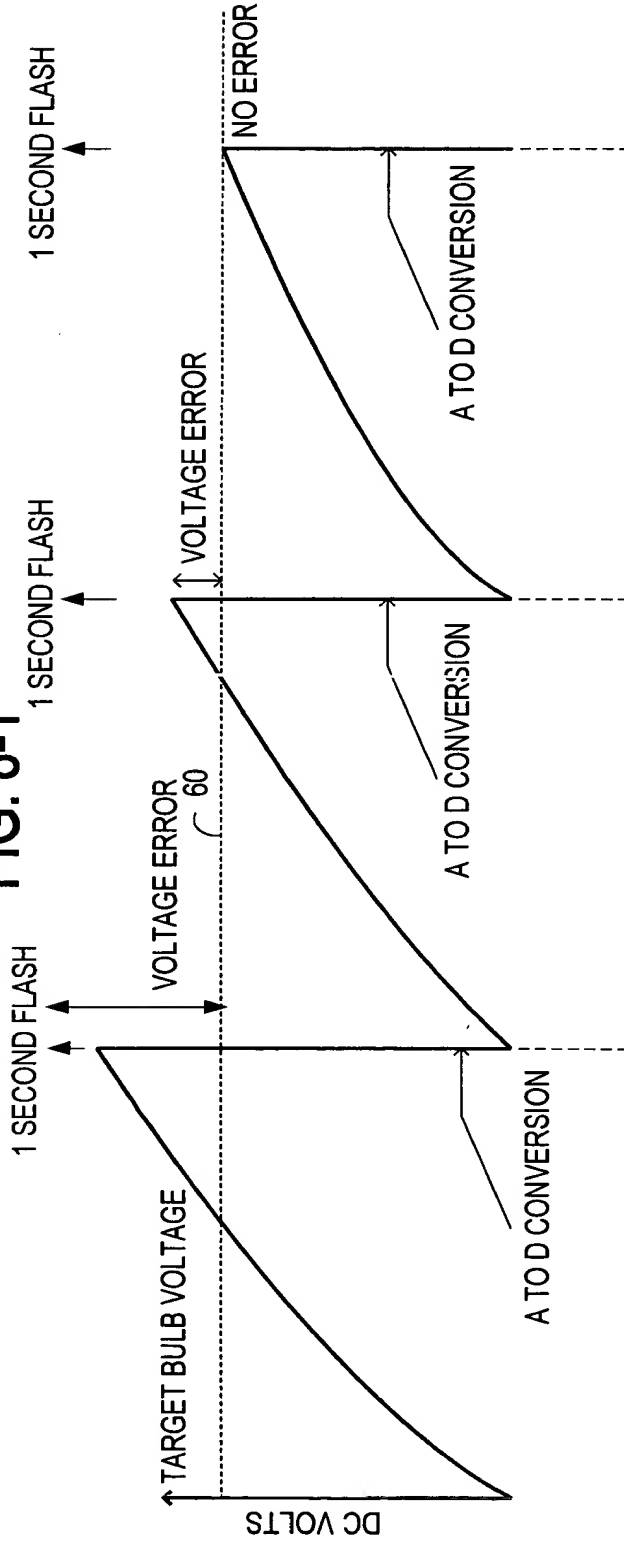
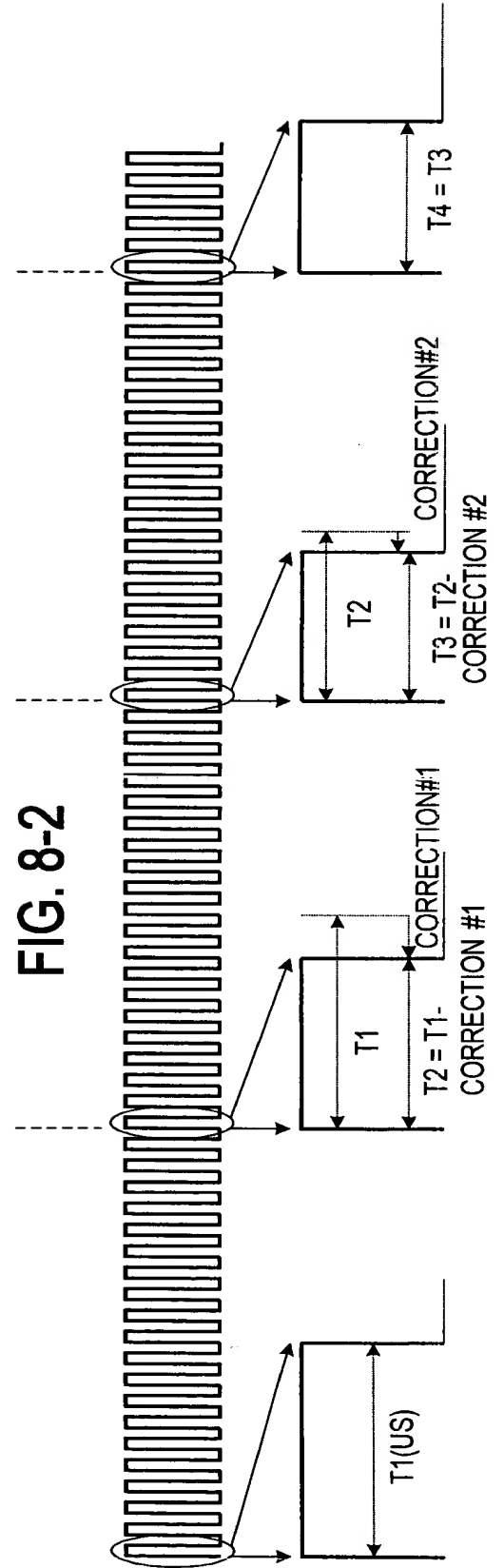


FIG. 8-2



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FIG. 9

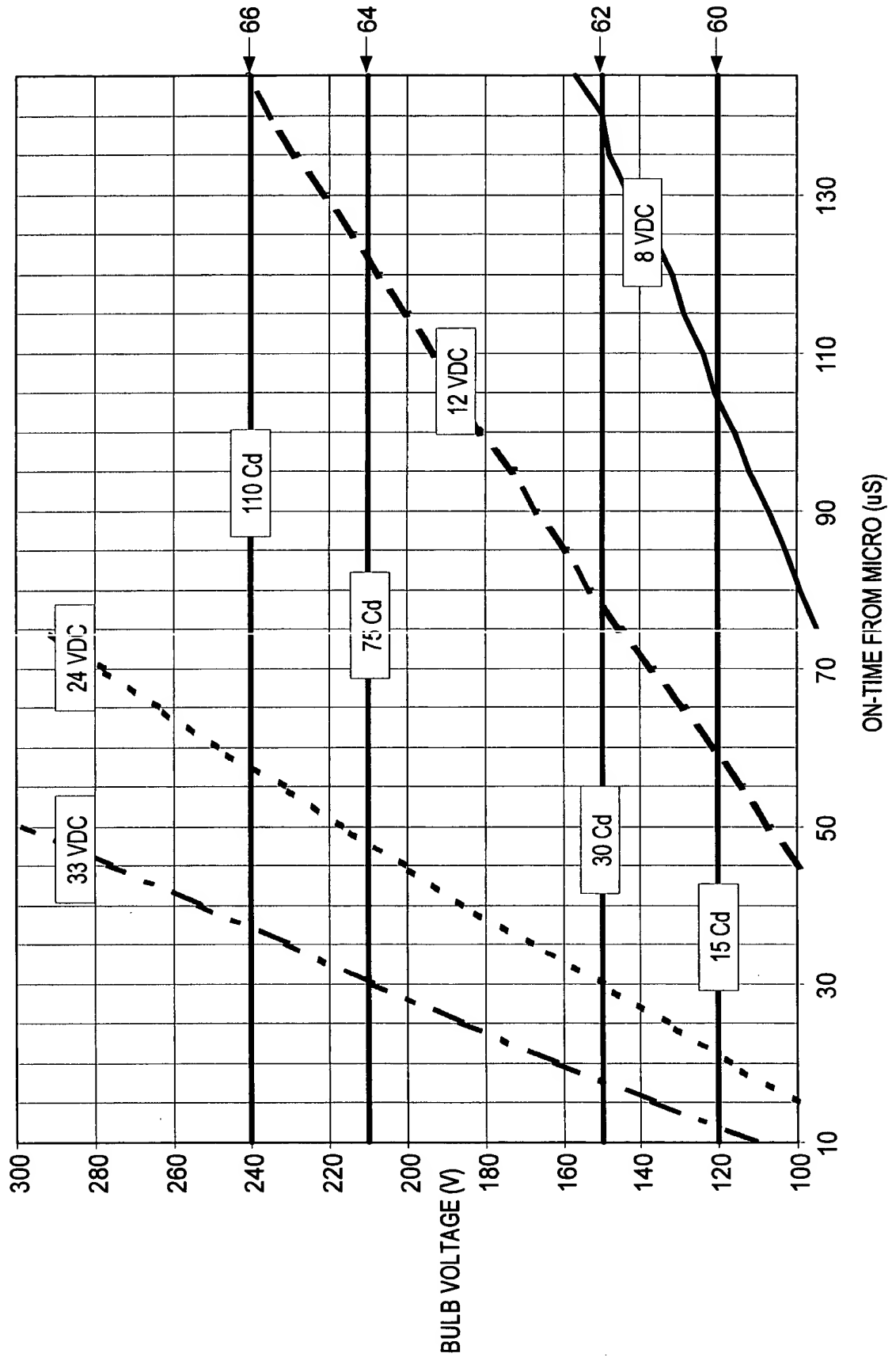
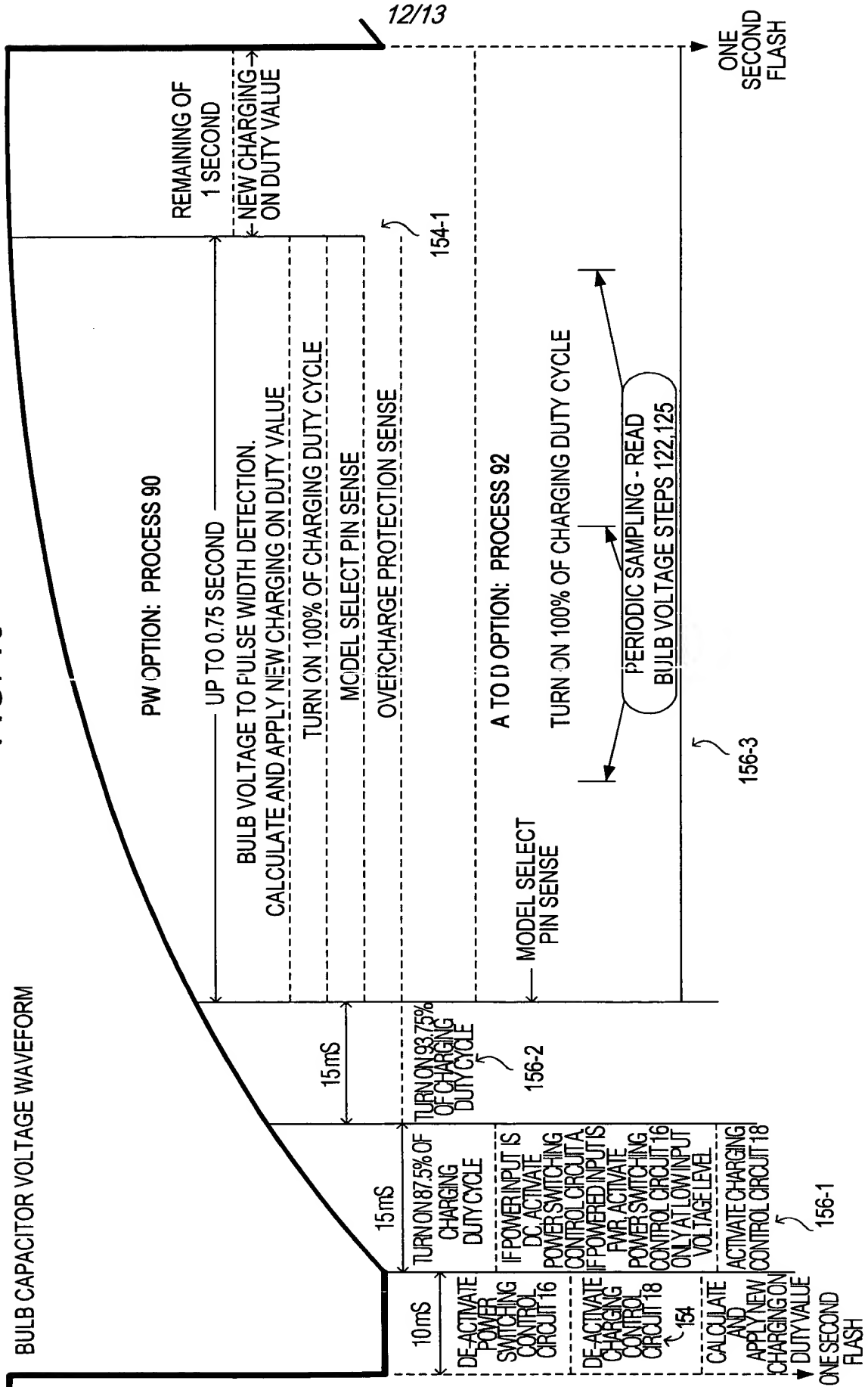


FIG. 10



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FIG. 11

